A Novel Approach for High Performance Slew Rate

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ABSTRACT

In this paper a research is proposed to enhance the slew rate using current mirror circuit and cascaded folded amplifier. Most slew rate enhancement circuits can either be used in current-mirror amplifier or folded-cascade amplifier, but not in both amplifiers. This circuit is implemented on AMS .65µm cmos process using a current mirror circuit with cascaded folded amplifier has very improved slew rate.

KEYWORD*- Amplifier, Load Capacitance, Slew rate Enhancement circuit, Transient Response*

I. INTRODUCTION

For the applications of low-power high-speed switched capacitor circuits, fast settling time of an operational amplifier is a common and critical requirement. The settling time of an amplifier can be divided into the slewing period and the quasi-linear period. In particular, the quasi-linear period depends on the small-signal behavior of the amplifier while the slewing period depends on the large-signal behavior. The settling time of these amplifiers is dominated and restricted by its slewing period as the maximum available current Imax to charge up the loading capacitor is limited in low power condition. The slew rate (SR) of single-stage amplifiers is given by

SR = Imax/CL

There are many works proposed to improve the slew rate using the idea of dynamic bias. Degrauwe proposed adaptive biasing based on circuit subtractors and current mirrors with gained ratio on the differential amplifier, so that the adaptive bias circuit is enabled to increase the bias current of the tail current source when there is a transient signal at the input. However, perfect current subtraction cannot be achieved due to mismatch of the current mirror at different operation regions. As a result extra offset voltage is a critical point of this design.[1]

1.1.Single Stage Amplifier- MOS transistors are capable of providing useful amplification in three different configurations. In the common-source configuration, the signal is applied to the base or gate of the transistor and the amplified output is taken from the drain. In the common-drain configuration, the signal is applied to the base or gate and the output signal is taken from the source. This configuration is often referred to as the source follower. In the common-base or common-gate configuration, the signal is applied to the emitter or the source, and the output signal is taken from the collector or the drain. Each of these configurations provides a unique combination of input resistance, output resistance, voltage gain, and current gain.

1.2.Common-Source Configuration

The resistively loaded common-source (CS) amplifier configuration is shown in Fig. 1(a) using an n-channel MOS transistor. The corresponding small-signal equivalent circuit is shown in Fig.1(b). As in the case of the bipolar transistor, the MOS transistor is cutoff for Vi = 0 and thus Id = 0 and Vo = VDD. As Vi is increased beyond the threshold voltage Vt, nonzero drain current flows and the transistor operates in the active region(which is often called as saturation for MOS transistors) when Vo > VGS-Vt.

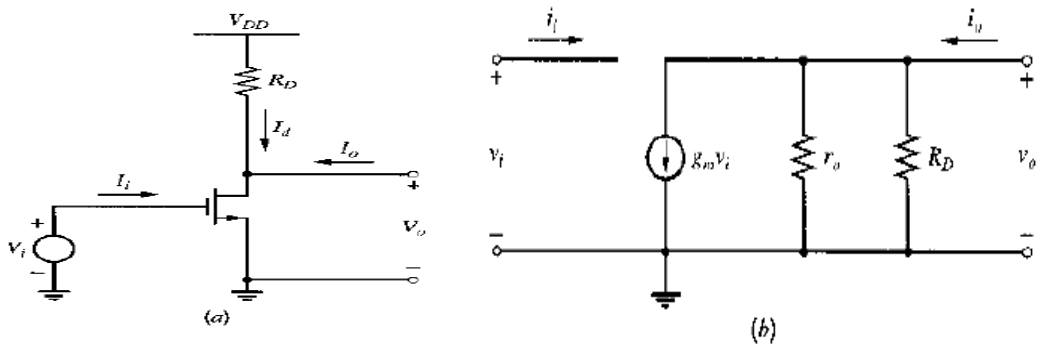

Figure.1 (a) Resistively loaded, common-source amplifier (b)Small-signal equivalent circuit

$$V_o = V_{DD} - I_d R_D$$
$$= V_{DD} - \frac{\mu_n C_{ox}}{2} \frac{W}{L} R_D (V_i - V_t)^2$$

The output voltage is equal to the drain-source voltage and decreases as the input increases. When Vo < VGS – Vt, the transistor enters the triode region, where its output resistance becomes low and the small-signal voltage gain drops dramatically.

Fig.2. shows the voltage characteristics of the circuit.The slope of this transfer characteristic at any operating point is the small-signal voltage gain at that point. The MOS transistor has much lower voltage gain in the active region than does the bipolar transistor, therefore the active region for the MOS CS amplifier extends over a much larger range of Vi than in the bipolar common-emitter amplifier.

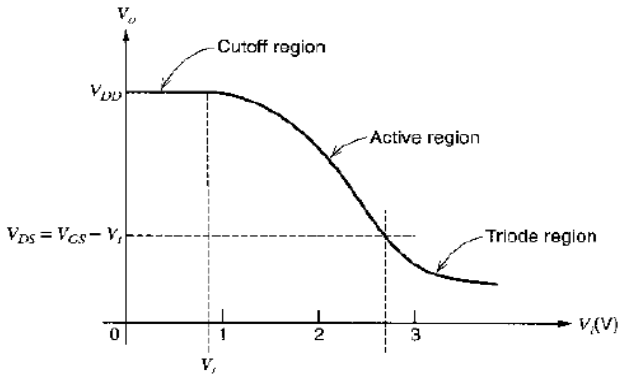

Figure.2 Output voltage versus input voltage for the common-source circuit.

The transconductance G_m is

$$G_m = \left.\frac{i_o}{v_i}\right|_{v_o = 0} = g_m$$

$$R_i = \frac{v_i}{i_i} \rightarrow \infty$$

Input resistance

Output resistance seen looking into output with input shorted,

$$R_o = \left.\frac{v_o}{i_o}\right|_{v_i=0} = R_D \parallel r_o$$

The open-circuit voltage gain is,

$$a_v = \left.\frac{v_o}{v_i}\right|_{i_o=0} = -g_m(r_o \parallel R_D)$$

1.3.Current-Mirror with Static-Bias and Dynamic-Bias

By using the static-bias and dynamic-bias a very high slew-rate current- mirror CMOS op-amp can be designed. It uses a circuit to inject an extra bias current into a conventional source coupled CMOS differential input stage in the presence of large differential signals. This measure substantially increases the slew-rate of an operational-amplifier for a given quiescent current.

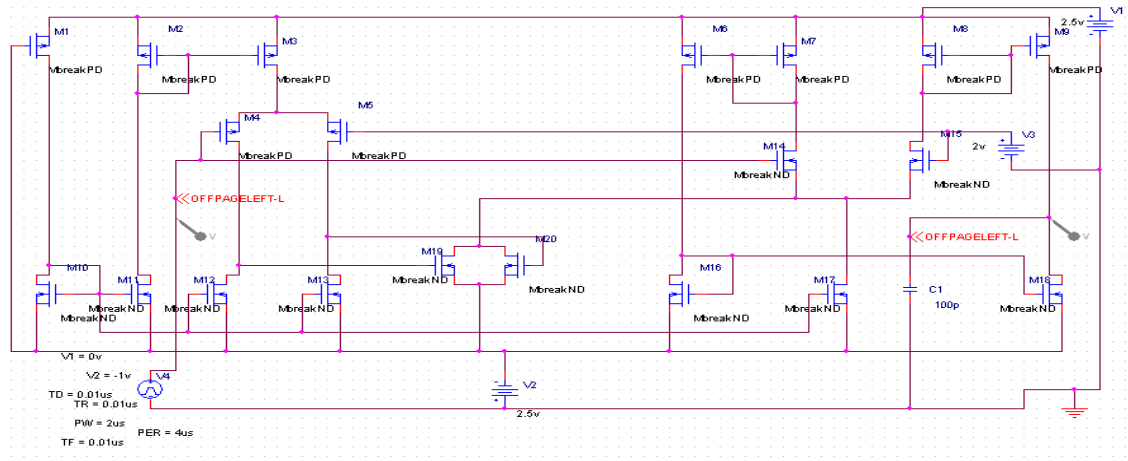

Figure.3. Current-mirror with static-bias and dynamic-bias.

Transient Analysis of current-mirror with static and dynamic bias

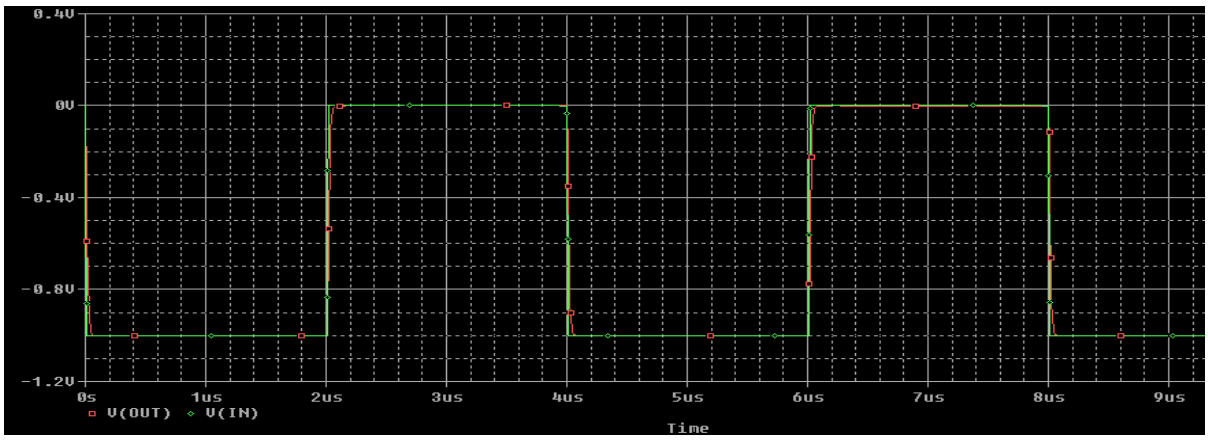

Figure 4 Transient analysis of CM with static and dynamic.

II. CURRENT-MIRROR SRE CIRCUIT

The technique at the active load device of the core amplifier is used to sense the fast signal transient. The simple SRE circuit is used as a plug-in feature to the core amplifier and do not affect its original small signal frequency response. Fig5,shows the circuit-

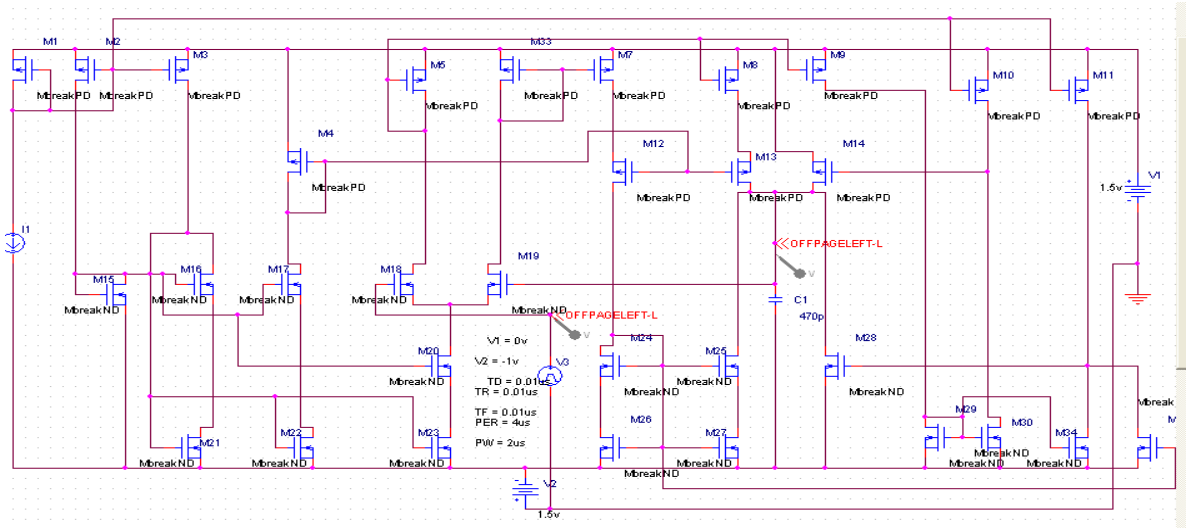

Figure.5 Current-mirror with SRE circuit.

III. CONCUSION

In the future technology has change rapidly, primarily to the larger unity-gain frequency and slew rate, the current-mirror OpAmp may be preferred over the folded-cascode OpAmp. However, one has to be careful that the current-mirror OpAmp has larger input noise as well, as its input stage is biased at a lower portion of the total bias current and therefore a relatively smaller gm given the same power consumption.In the previous work we know that large capacitive load decreases slewing rate if we increase of biasing current which increases the static current loss in the amplifier circuit.

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